WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate in which surface is formed a depression having a closed figure when viewed from the substrate normal; and

a semiconductor layer which is formed on said surface of said substrate by crystal growth from at least an inside face of said depression.

2. The semiconductor device of claim 1,

wherein said depression includes at least two adjacent inside faces unparallel to said surface of said substrate; and

wherein an angle, formed by two line segments created by intersecting of said two inside faces and a plane parallel to said surface of said substrate, is either 60 degrees or 120 degrees.

3. The semiconductor device of claim 2,

wherein said figure of said depression is either substantially an equilateral triangle or substantially an equilateral hexagon.

4. The semiconductor device of claim 2,

wherein said substrate comprises a semiconductor layer having a hexagonal crystal structure; and

wherein said depression is formed in a surface of said semiconductor layer.

5. The semiconductor device of claim 4,

wherein said semiconductor layer constituting said substrate and said semiconductor layer formed on said surface of said substrate each comprise nitride semiconductor.

6. The semiconductor device of claim 4,

wherein said inside face of said depression is either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number, or its equivalent plane.

7. The semiconductor device of claim 6,

wherein said number n is 1.

8. The semiconductor device of claim 1,

wherein a plurality of said depressions are formed in said surface of said substrate.

9. The semiconductor device of claim 1,

wherein a plurality of semiconductor layers including at least an active layer are formed on said substrate.

10. A semiconductor device comprising:

a substrate on which surface is formed a projection; and

a semiconductor layer which is formed on said surface of said substrate by crystal growth from at least a side face of said projection;

wherein said projection includes at least two adjacent side faces unparallel to said surface of said substrate; and

wherein an angle, formed by two line segments created by intersecting of said two side faces and a plane parallel to said surface of said substrate, is either 60 degrees or 120 degrees.

11. The semiconductor device of claim 10,

wherein said substrate comprises a semiconductor layer having a hexagonal crystal structure; and

wherein said projection is formed on a surface of said semiconductor layer.

12. The semiconductor device of claim 11,

wherein said semiconductor layer constituting said substrate and said semiconductor layer formed on said surface of said substrate each comprise nitride semiconductor.

13. The semiconductor device of claim 11,

wherein said side face of said projection is either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number, or its equivalent plane.

14. The semiconductor device of claim 13,

wherein said number n is 1.

15. The semiconductor device of claim 10,

wherein a plurality of said projections are formed on said surface of said substrate.

16. The semiconductor device of claim 10,

wherein a plurality of semiconductor layers including at least an active layer are formed on said substrate.

17. A method for the manufacture of a semiconductor device comprising:

a step of preparing a substrate in which surface is formed a depression having a closed figure when viewed from the substrate normal; and

a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure.

18. A method for the manufacture of a semiconductor device comprising:

a step of preparing a substrate;

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a step of forming on a surface of said substrate a depression having a closed figure when viewed from the substrate normal; and

a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure.

19. The manufacture method of claim 18,

wherein said depression forming step is performed such that an inside face of said depression is defined by either a plane having a plane orientation of (1, -1, 0, 1) or its equivalent plane.

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20. The manufacture method of claim 19,

wherein said depression forming step is the step of forming on said major surface of said substrate defined by a (0, 0, 0, 1) plane a depression having a bottom face whose figure is either an equilateral triangle or an equilateral hexagon.

21. The manufacture method of claim 17,

wherein said semiconductor layer forming step is the step of forming a semiconductor layer in which an inside face of said depression serves as a crystal growth surface.

22. The manufacture method of claim 21,

wherein said semiconductor layer forming step includes a step in which said semiconductor layer crystal grows in a vertical direction from said inside face of said depression.

23. The manufacture method of claim 18,

wherein said semiconductor layer forming step is the step of forming a semiconductor layer in which an inside face of said depression serves as a crystal growth surface.

24. The manufacture method of claim 23,

wherein said semiconductor layer forming step includes a step in which said semiconductor layer crystal grows in a vertical direction from said inside face of said depression.

25. The manufacture method of claim 17,

wherein said semiconductor layer forming step is the step of forming a layer which comprises Group III nitride-based compound semiconductor.

26. The manufacture method of claim 18,

wherein said semiconductor layer forming step is the step of forming a layer which comprises Group III nitride-based compound semiconductor.

27. The manufacture method of claim 25,

wherein said Group III nitride-based compound semiconductor layer is grown by a metal organic vapor epitaxy method.

28. The manufacture method of claim 26,

wherein said Group III nitride-based compound semiconductor layer is grown by a metal organic vapor epitaxy method.

29. The manufacture method of claim 18,

wherein said substrate preparing step is the step of preparing a sapphire substrate on which surface is formed a Group III nitride-based compound semiconductor layer; and

wherein said depression forming step is the step of forming said depression in a surface of said Group III nitride-based compound semiconductor layer.

30. A semiconductor substrate comprising:

a substrate in which surface is formed a depression having a closed figure when viewed from the substrate normal; and

a semiconductor layer which is formed on said surface of said substrate by crystal growth from at least an inside face of said depression.

31. The semiconductor substrate of claim 30,

wherein said depression includes at least two adjacent inside faces unparallel to said surface of said substrate; and

wherein an angle, formed by two line segments created by intersecting of said two inside faces and a plane parallel to said surface of said substrate, is either 60 degrees or 120 degrees.

32. The semiconductor substrate of claim 31,

wherein said figure of said depression is either substantially an equilateral triangle or substantially an equilateral hexagon.

33. The semiconductor substrate of claim 31,

wherein said substrate comprises a semiconductor layer having a hexagonal crystal structure; and

wherein said depression is formed in a surface of said semiconductor layer.

34. The semiconductor substrate of claim 33,

wherein said semiconductor layer constituting said substrate and said semiconductor layer formed on said surface of said substrate each comprise nitride semiconductor.

35. The semiconductor substrate of claim 33,

wherein said inside face of said depression is either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number, or its equivalent plane.

36. The semiconductor substrate of claim 35,

wherein said number n is 1.

37. The semiconductor substrate of claim 30,

wherein a plurality of said depressions are formed in said surface of said substrate.

38. A semiconductor substrate comprising:

a substrate on which surface is formed a projection; and

a semiconductor layer which is formed on said surface of said substrate by crystal growth from at least a side face of said projection;

wherein said projection includes at least two adjacent side faces unparallel to said surface of said substrate; and

wherein an angle, formed by two line segments created by intersecting of said two side faces and a plane parallel to said major surface of said substrate, is either 60 degrees or 120 degrees.

39. The semiconductor substrate of claim 38,

wherein said substrate comprises a semiconductor layer having a hexagonal crystal structure; and

wherein said projection is formed on a surface of said semiconductor layer.

40. The semiconductor substrate of claim 39,

wherein said semiconductor layer constituting said substrate and said semiconductor layer formed on said surface of said substrate each comprise nitride semiconductor.

41. The semiconductor substrate of claim 40,

wherein said side face of said projection is either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number, or its equivalent plane.

42. The semiconductor substrate of claim 41,

wherein said number n is 1.

43. The semiconductor substrate of claim 38,

wherein a plurality of said projections are formed on said surface of said substrate.

44. A method for the manufacture of a semiconductor substrate including:

a step of preparing a substrate for crystal growth;

a step of depositing on said crystal growth substrate a first semiconductor layer having a hexagonal crystal structure;

a step of exposing either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number, or its equivalent plane by subjecting a part of said first semiconductor layer to an etching process; and

after said exposing step, a step of depositing on said first semiconductor layer a second semiconductor layer having a hexagonal crystal structure.

45. The manufacture method of claim 44,

said exposing step including:

a step of applying onto said first semiconductor layer a resist pattern having an opening whose figure is either substantially an equilateral triangle, or substantially an

equilateral hexagon when viewed from the substrate normal; and

a step of forming a depression by subjecting said first semiconductor layer to an etching process in which said resist pattern is used as a mask so that said depression has an inside face comprising either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number, or its equivalent plane.

46. The manufacture method of claim 45,

wherein said resist pattern has a plurality of said openings arrayed at equal intervals.

47. The manufacture method of claim 44,

said exposing step including:

a step of applying onto said first semiconductor layer a resist pattern whose figure is either substantially an equilateral triangle, or substantially an equilateral hexagon when viewed from the substrate normal; and

a step of forming a projection by subjecting said first semiconductor layer to an etching process in which said resist pattern is used as a mask so that said projection has a side face comprising either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number or its equivalent plane.

48. The manufacture method of claim 47,

wherein said resist pattern comprises a plurality of said resist patterns arrayed at equal intervals.

49. A method for the manufacture of a semiconductor substrate comprising:

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a step of forming a substrate having on a surface thereof a depression having a closed figure when viewed from the substrate normal;

a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure; and

a step of taking out said semiconductor layer by removal of said substrate.

50. The manufacture method of claim 49,

wherein said depression has an inside face defined by either a plane having a plane orientation of (1, -1, 0, 1) or its equivalent plane.

51. The manufacture method of claim 50,

wherein said depression has, in said major surface of said substrate defined by a (0, 0, 0, 1) plane, a bottom face whose figure is either an equilateral triangle or an equilateral hexagon.

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52. A method for the manufacture of a semiconductor substrate comprising:

a step of forming a substrate having on a surface thereof a projection;

a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure; and

a step of taking out said semiconductor layer by removal of said substrate.

53. The manufacture method of claim 52,

wherein said projection has a side face defined by either a plane having a plane orientation of (1, -1, 0, 1) or its equivalent plane.

54. The manufacture method of claim 52,

wherein said projection has, in said major surface of said substrate defined by a (0, 0, 0, 1) plane, a bottom face whose figure is either an equilateral triangle or an equilateral hexagon.

55. The manufacture method of claim 49,

wherein said semiconductor layer forming step is the step of forming a layer of Group III nitride-based compound semiconductor.

56. The manufacture method of claim 52,

wherein said semiconductor layer forming step is the step of forming a layer of Group III nitride-based compound semiconductor.

57. The manufacture method of claim 55,

wherein said Group III nitride-based compound semiconductor layer is grown by hydride vapor phase epitaxy.

58. The manufacture method of claim 56,

wherein said Group III nitride-based compound semiconductor layer is grown by hydride vapor phase epitaxy.

59. The manufacture method of claim 49,

said substrate forming step including:

a step of preparing a sapphire substrate; and

a step of forming on said sapphire substrate a Group III nitride-based compound semiconductor layer having said depression in a surface thereof.

60. The manufacture method of claim 52,

said substrate forming step including:

a step of preparing a sapphire substrate; and

a step of forming on said sapphire substrate a Group III nitride-based compound semiconductor layer having said projection on a surface thereof.

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